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10/043,047	01/09/2002	Chang-Sik Yoo	SAM-0204	5014

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/043,047	YOO ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *54-56,65-71,73-80 and 87-114* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *54-56 and 65* is/are allowed.

6)☒ Claim(s) *66-71,73-80 and 87-114* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 66-67, 73-79, 91, 93-96, 101-104, 106, 107, 109, 110, 112-114 are rejected under 35 U.S.C. 102(e) as being anticipated by Gillingham et al., US Patent 6510503, hereinafter Gillingham.

3. In re claim 66, Gillingham discloses a memory system [80] having a stub configuration [col.10, l.58 – col.11, l.8] comprising:

- A controller [82] for generating a first clock signal [86], a control signal [e.g., row], an address signal [e.g., col] [col.3, ll.1-12] and data signals on a first clock signal line, a control signal line, and address signal line and a data bus, respectively [col.10, l.10 – col.11, l.8; col.12, ll.1-12; fig.7].
- A first memory module [170] including at least one memory device [100, 174] connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a control/address buffer device [106, 107, 108 with associated circuitry] that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to

the at least one memory device in response to the first clock signal [fig.8a; control and address signal being supplied to core dram memory device 100].

- The first memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the at least one memory device in synchronization with the first clock signal [col.10, ll.49-53; uses 86 to write data].
- The first memory module, in response to the read command, initiating a read operation for reading data from the at least one memory device to the data bus, and the control/address buffer device generating a second clock signal [outclk, dclk] in response to the first clock signal, the second clock signal being provided to the controller on a second clock signal line that is separate from the first clock signal line [86, clk propagates from controller to module and dclk propagates from module to controller in a read operation], the controller receiving the data signals on the data bus in response to the second clock signal during the read operation [col.10, ll.40-57; col.11, ll.23-49].

4. As to claims 67, 96, 107, Gillingham discloses, wherein the memory system further includes a second memory module, the first and second memory modules generating respective first and second independent return clock signals as the second clock signal [170 corresponds to 84 each with its own clock generators of dclk], and further comprising a motherboard coupling the first and second memory modules and the controller, the motherboard including the data bus, the control signal line, the address signal line, the first clock signal line and first and second independent return clock signal lines for transfer of the first and second return clock signals form the first and second memory modules to the controller [fig.7, 8a, 8c, 13].

5. As to claims 74, 102, 109, Gillingham discloses, wherein the system comprises multiple memory modules and wherein the multiple memory modules each generate independent second clock signals, the second clock each being different in phase relative to each other [col.13, ll.39-54; phase differences require synchronization].

6. As to claims 75, 103, Gillingham discloses, wherein the phases of the multiple second clock signals are different in phase due to the difference in propagation delay between each of the memory modules and the controller [col.2, ll.42-44, ll.59-60; memory modules situated at different distances induce different propagation delays].

7. As to claims 76, 104, Gillingham discloses, wherein the propagation delay of the second clock signal on the second clock signal line from the first memory module to the controller is substantially equal to that of the data signals on the data bus [col.2, ll.36-38].

8. As to claims 77, 94, 113, Gillingham discloses, wherein the control/address buffer device or clock return further includes a phase locked loop that receives the first clock signal and generates the second clock signal in response to the first clock signal [col.2, ll.10-13].

9. As to claims 78, 95, 114, Gillingham discloses, wherein the control/address buffer device or clock return further includes a delay locked loop that receives the first clock signal and generates the second clock signal in response to the first clock signal [col.2, ll.10-13].

10. As to claim 79, Gillingham discloses, wherein the control/address buffer device includes a return path that is coupled to a first clock signal line that receives the first clock signal for generating the second clock signal in response to the first clock signal [fig.6a; cfc loops to ctc].

11. In re claim 91, Gillingham discloses a memory system [80] having a stub configuration [col.10, l.58 – col.11, l.8] comprising:

- A controller [82] for generating a first clock signal [86], a control signal [e.g., row], an address signal [e.g., col] [col.3, ll.1-12] and data signals on a first clock signal line, a control signal line, and address signal line and a data bus, respectively [col.10, l.10 – col.11, l.8; col.12, ll.1-12; fig.7].
- A first memory module [170] including at least one memory device [100, 174] connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return [106, 107, 108 with associated circuitry] that is coupled to the first clock signal line that receives first clock signal, and a control/address buffer device [106, 107, 108 with associated circuitry] receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal [fig.8a; control and address signal being supplied to core dram memory device 100 with reception of first clock signal].
- The first memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the at least one memory device in synchronization with the first clock signal [col.10, ll.49-53; uses 86 to write data].
- The first memory module, in response to the read command, initiating a read operation for reading data from the at least one memory device to the data bus, and the clock return providing a second clock signal [outclk, dclk] in response to the first clock signal, the second clock signal being provided to the controller on a second clock signal line that is separate from the first clock signal line [86, clk propagates from controller to module and dclk propagates from module to controller in a read operation], the controller receiving

the data signals on the data bus in response to the second clock signal during the read operation [col.10, ll.40-57; col.11, ll.23-49].

12. As to claims 93, 112, Gillingham discloses, wherein the first memory module further includes a control/address buffer device [106] that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal [fig.8a].

13. In re claim 106, Gillingham discloses each and every limitation as discussed above in reference to claim 66. Gillingham discloses the memory system; therefore, Gillingham discloses the method of operating the memory system.

14. In re claim 110, Gillingham discloses each and every limitation as discussed above in reference to claim 91. Gillingham discloses the memory system; therefore, Gillingham discloses the method of operating the memory system.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 68, 97, 108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham as applied to claims 67, 96, 107 above, and further in view of Wada et al., US Patent 5379248, hereinafter Wada.

17. Gillingham taught each and every limitation as discussed above. Gillingham did not disclose explicitly that the first and second return clock signal lines are crossed on the motherboard between the first and second modules.

18. Wada discloses a memory system wherein a first and second signal lines [bit lines] are crossed between a first and second modules [peripheral circuits] [abstract].

19. It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham and Wada before him at the time the invention was made, to modify the memory system taught by Gillingham to include the teachings of Wada, in order to obtain the memory system wherein the first and second return clock signal lines are crossed on the motherboard between the first and second modules. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase the freedom of circuit line layout [Wada: abstract].

20. Claims 69-71, 87-89, 98-100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham as applied to claims 11and 66 above, and further in view of Yoshitake, US Patent 6043704.

21. Gillingham taught each and every limitation as discussed above. Gillingham did not discuss the details of a dummy load regarding the memory modules [Gillingham: col.13, ll.20-37; col.15, l.60 – col.16, l.46].

22. In re claims 69 and 98, Yoshitake discloses a system wherein a return clock signal line [clock wiring line] is coupled to a dummy load [31] [col.10, ll.56-64].

23. It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham and Yoshitake before him at the time the invention was made, to modify the memory

system taught by Gillingham to include the teachings of Yoshitake, in order to obtain the memory system wherein the first return clock signal line is coupled to a dummy load on the second memory module and wherein the second return clock signal line is coupled to a dummy load on the first memory module. One of ordinary skill in the art would have been motivated to make such a combination as it provides a very well known way to correct clock skews [Yoshitake: col.10, ll.56-64] and match input capacitance [Gillingham: col.13, ll.20-37].

24. As to claims 70, 88, 99, Yoshitake discloses, wherein the dummy load comprises a load capacitor or a dummy pin [col.10, ll.56-64; 31 contains capacitance load].

25. As to claims 71, 100, Yoshitake discloses, wherein the dummy load is selected to match the capacitance loading of a data bus [multiple clock wiring lines constitute a bus as is well known in the art] [col.10, ll.56-64; 31 adjusted to match capacitance in order to adjust skew].

26. As to claim 87, Yoshitake discloses, comprising a module [second buffers] mounted to a first side of a memory module [10 contains RAM], and further comprising a dummy load [31] for coupling to a first signal line of the module to provide load matching with a load experienced by a second signal line of memory devices [third buffers] mounted to both first and second sides of the memory module [col.3, l.54 – col.5, l.63; col.10, ll.56-64].

27. As to claim 89, Yoshitake discloses, wherein the first signal line comprises the first clock signal line or the second clock signal line, and wherein the second signal line comprises the data bus or the first clock signal line [col.3, l.54 – col.5, l.63; col.10, ll.56-64].

28. Claims 80, 92, 111 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham as applied to claims 79, 91, 110 above, and further in view of Moyal et al., US Patent 6326853, hereinafter Moyal.

29. Gillingham taught each and every limitation as discussed above in reference to claim 9. Gillingham did not discuss the details of the memory module regarding capacitors.

30. Moyal discloses a system comprising a capacitor having a capacitance that is selected to compensate for capacitive loading; the capacitor being coupled to a junction of a signal line and a return path [fig.4; col.2, ll.1-11].

31. It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham and Moyal before him at the time the invention was made, to modify the memory system taught by Gillingham to include the teachings of Moyal, in order to obtain the memory system wherein the memory module further includes a capacitor having a capacitance that is selected to compensate for capacitive loading on the data bus by the memory device of the memory module; the capacitor being coupled to a junction of the first clock signal line and the return path. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce phase mismatches [Moyal: col.2, ll.1-11].

32. Claims 90, 105 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham as applied to claim 66 above, and further in view of Keeth, US Patent 6029250.

33. Gillingham taught each and every limitation as discussed above. Gillingham did not discuss the details of clock generations in the memory module.

34. Keeth discloses a memory system [fig.4] comprising a memory module [404], in response to a read command, initiating a read operation for reading data from memory devices [80a-h] to a data bus [dq] in synchronization with a first clock signal [rclk] and generating a second clock signal [dclk0/1] in response to the first clock signal, the data signals and the second clock signal being output from the memory module in synchronization with the first clock signal

[fig.5; dclk in sync with rclk; data in sync with dclk in order to be latched correctly], the second clock signal being provided to a controller [402], the controller receiving the data signals on the data bus in response to the second clock signal during the read operation [col.10, ll.26-39; col.13, ll.8-23, l.40 – col.15, l.14].

35. It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham and Keeth before him at the time the invention was made, to modify the memory module taught by Gillingham to include the teachings of Keeth, in order to obtain the memory system comprising during the read operation, the data signals and the second clock signal are output from the first memory module in synchronization with the first clock signal. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better synchronize memory access of increasing number of memory modules [Keeth: col.1, l.17 – col.2, l.14; col.7, ll.28-52].

Allowable Subject Matter

36. Claims 54-56, 65 are allowed.

Response to Arguments

37. Applicant's arguments regarding claims 66 and similar have been fully considered but they are not persuasive. Applicant argues that Gillingham does not teach "the control/address buffer device... is included in the 'first memory module' and services any or all of the at least one memory devices on the module by supplying the 'control signal and the address signal' to each of the 'at least one memory device' on the module 'in response to the first control signal'". Examiner disagrees and submits that Gillingham does disclose the control/address buffer device [106, 107, 108 with associated circuitry] that is included in the first memory module [170] and

services any or all of the at least one memory devices [100, 174] on the module by supplying the control signal and the address signal to the at least one memory device on the module [fig.8a].

Conclusion

38. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
January 17, 2007

A. ELAMIN
PRIMARY EXAMINER